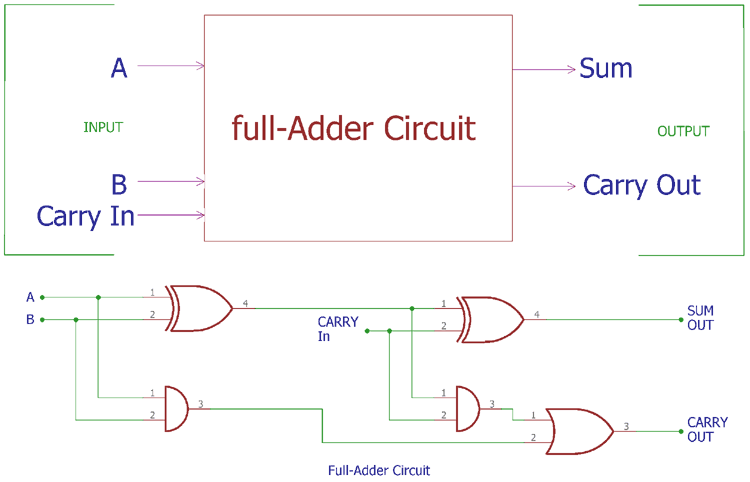
EXPERIMENT NO : 4

## Write a Verilog code for the implementation of full adder using instance

NAME : SAHIL TRIPATHI

FULL ADDER



FULL ADDER FULL INSTANCE

module FA(a,b,cin,sum,cout);

input a,b,cin;

output sum,cout;

wire x,y,z;

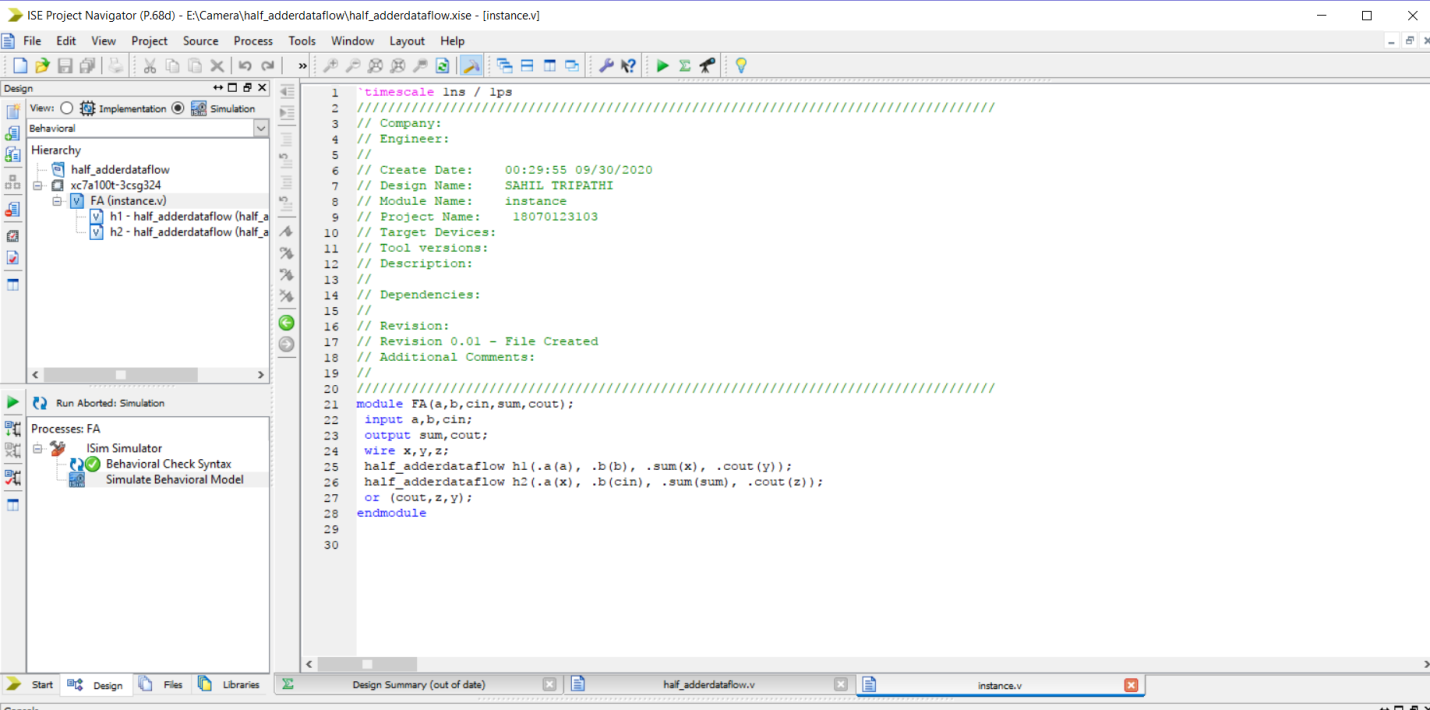
half\_adderdataflow h1(.a(a), .b(b), .sum(x), .cout(y));

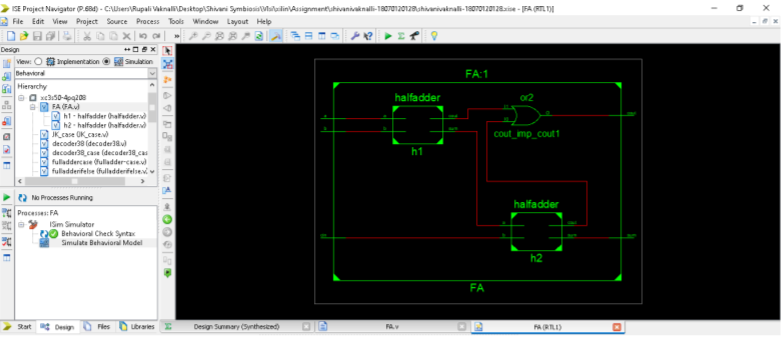
half\_adderdataflow h2(.a(x), .b(cin), .sum(sum), .cout(z));

or (cout,z,y);

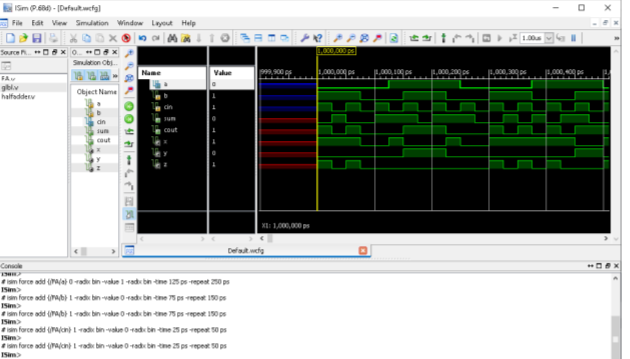
endmodule

IMAGE OF CODE-



RTL SCHEMATICS

SIMULATION



SO HENCE I HAVE LEARNED HOW TO SIMULATE FULL ADDER INSTANCE USING HALF ADDER IN XILIN SOFTWARE